CLAIMS

What is claimed is:

1. A method comprising:

receiving a request to read a modified cache line at a responding node of a shared memory multiprocessor architecture from a requesting node of the shared memory multiprocessor architecture;

transmitting a response to the request by substantially simultaneously instructing a switch coupled to the responding node, the requesting node and a home node, to update a memory at the home node with data read from the modified cache line and provide an answer to the requesting node, wherein the home node is different from the responding node.

2. The method of claim 1, wherein the answer includes a copy of the data read from the modified cache line.

3. The method of claim 1, wherein the response further provides information regarding a state transition of the modified cache line.

4. The method of claim 3, wherein the information regarding a state transition indicates whether the modified cache line is transitioning from a modified state to an invalid state or from a modified state to a shared state.

5. The method of claim 1, further comprising updating the memory at the home node.

6. The method of claim 5, further comprising providing a completion response to the requesting node.

7. The method of claim 3, wherein the status indicates a cache coherence protocol type used by the responding node.

8. A shared memory multiprocessor system comprising:

a plurality of node controllers and a switch coupled to each of the plurality of node controllers configured to

transmit a read request regarding a modified cache line from a first node controller of the plurality of node controllers through the switch to a second node controller of the plurality of node controllers, wherein the second node controller is distinct from the first node controller; and

in response to receiving the read request regarding the modified cache line, the second node controller instructs the switch to update a home memory residing exclusively on a third node controller of the plurality of node controllers.

9. The shared memory multiprocessor system of claim 8 wherein the switch maintains a presence vector.

10. The shared memory multiprocessor system of claim 9 wherein the presence vector maintains a status of a cache line for each participating node controller of the plurality of node controllers.

11. The shared memory multiprocessor system of claim 10 wherein the presence vector indicates if the cache line for each corresponding participating node controller contains a copy of a contents stored in the home memory.

12. A method comprising a responding node initiating an implicit write-back in response to a read request directed to a modified cache line at the responding node.

13. The method of claim 12, wherein the implicit write-back includes information causing a switch to answer the read request and update a home memory.

14. The method of claim 12, wherein the implicit write-back further includes information identifying a state of the modified cache line targeted by the read request.

15. A machine-readable medium having stored thereon data representing sequences of instructions, the sequences of instructions which, when executed by a processor, cause the processor to:

receive a request to read a cache line at a responding node of a shared memory multiprocessor architecture from a requesting node of the shared memory multiprocessor architecture;

transmit a response to the request by substantially simultaneously instructing a switch coupled to the responding node, the requesting node and a home node, to update a memory at the home node with data read from the cache line and provide an answer to the requesting node, wherein the home node is different from the responding node.

16. The machine-readable medium of claim 15 wherein the answer includes a copy of the data read from the cache line.

17. The machine-readable medium of claim 15, wherein the response further provides a status of the cache line.

18. The machine-readable medium of claim 17, wherein the status indicates whether the cache line is transitioning from a modified state to an invalid state or from a modified state to a shared state.

19. The machine-readable medium of claim 15, wherein the sequence of instructions further causes the processor to update the memory at the home node.

20. The machine-readable medium of claim 19, wherein the sequence of instructions further causes the processor to provide a completion response to the requesting node.

21. The machine-readable medium of claim 17, wherein the status indicates a cache coherence protocol type used by the responding node.